Effect of Device Controlling Parameters on Organic Field Effect Transistors BGTC Configuration: An Experimental Study

Boyapally Sai Sharaj and Atul S. M. Tripathi

ABSTRACT

In recent years, the potential applications of organic field-effect transistors (OFETs) have attracted significant interest in flexible electronics, low-cost displays, and large-area sensor arrays. This research presents a detailed simulation study on the design and modeling of OFETs using organic semiconductor materials. The study primarily focuses on analyzing the electrical characteristics of devices by varying key parameters: channel length, dielectric thickness, dielectric materials, and drain voltage. Performance optimization is achieved by systematically examining how these parameters affect the OFETs' electrical behavior. The results highlight the significance of appropriate device design, material selection, and simulation-based optimization in achieving high-performance OFETs. The insights from this work contribute to the ongoing advancement of OFET technology and lay the foundation for future research in organic electronics.

Keywords: Organic field-effect transistor simulation, Bottom-gate top-contact architecture, High-k TA2O5 dielectric, Silvaco atlas tcad modeling, Pentacene active layer

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Introduction

When it comes to creating organic transistors (organic field-effect transistors [OFET]) have garnered considerable interest for applications in large-area electronics with low in fabrication cost, such as displays, flexible sensors, and in radio frequency identification tags.[1] Similar to a standard MOSFET, a fundamental component of contemporary integrated circuits, an OFET is a device that regulates a channel's conduction at the interface between a semiconductor and a dielectric by using an electric field.[2] The advent of MOSFET technology led to a prolonged period of dormancy for OFET technology.[3] OFET, consists of the semiconducting layer organic material, insulating layer to isolate the gate, and metal source drain contact electrode. Typically, thin-film, the organic semiconductor layer acts as the route for the charge carriers.[4] The source and drain electrodes inject and collect the charge carriers, while the gate electrode controls the conductivity of the channel by varying the charge carrier density. Due to its unique characteristics like flexibility of substrate, low-power applications, etc., OFET's are used in a variety of applications like flexible displays, smart card & RF-ID tags, E-paper, organic film memory, and more.[5] Numerous devices with various parameters were applied, and findings were documented. Due to its high mobility, pentacene the active layer of transistors utilized an organic semiconductor. The characteristics of the Bottom gate top contact (BGTC) configuration were simulated in this research.[6] The second section of the paper will address OFETs. It will cover the history and literature review, OFET and BGTC architectures, the value of TCAD simulation, device structure, and the parameters—channel length, dielectric thickness, dielectric materials, and drain voltage—that impact the device's performance. Implementing the OFET structure and comparing its properties for various device parameters will be done in section "Results and Discussion,"[7] and the conclusion will be presented in section "Conclusion".

Organic Thin Film Transistors

Survey of Literature and Background

Kumar et al. conducted a comparable study on Organic FET[3] and published a research paper in polymer reviews. "A review" provides a thorough overview of the latest advancements and obstacles in the area of organic thin film transistors (OTFTs). This Devices utilize organic materials in the active layer to regulate the movement of electric charges when an electric field is applied.

Their potential applications in large-area, flexible, low-cost, and printable electronics, such as displays, sensors, RFID tags, and logic circuits, have led to a significant interest in OTFTs.[3]

The article covers various aspects of OTFTs, such as:

- The fundamental operational concept and performance metrics of OTFTs, including field-effect mobility, current on/off ratio, threshold voltage, subthreshold slope, and stability.
- OTFT structures come in various types, including one and dual gate, each with its own set of importance.
- Polymers and small molecules are among the different organic materials utilized in the construction of OTFTs, along with their molecular structures, charge transport mechanisms, and doping methods.
- Depositing the organic layers can be achieved using various techniques, including spin coating, inkjet printing, thermal evaporation, and solution shearing, each of which can influence the morphology and crystallinity of the films.
- The different materials and methods for forming the dielectric layer, the electrodes, and the substrate of OTFTs, such as silicon oxide, organic insulators, metal oxides, metals, carbon nanotubes, graphene, glass, plastic, paper, and fabric.
- Different compact models are utilized to characterize the electrical performance of OTFTs and improve their design and functionality.
- OTFTs are being increasingly used in a variety of fields, including inverters, light emitting diodes, RFID tags, DNA sensors, and memory devices.

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The paper also discusses some of the current challenges and future directions for OTFT research and development. Some of the challenges include improving the mobility, stability, uniformity, reproducibility, noise margin, voltage swing, and subthreshold slope of OTFTs. Some of the future directions include exploring new organic materials with novel properties and functions; developing new fabrication techniques that are compatible with large-scale production; integrating OTFTs with other components to form complex circuits and systems; and demonstrating novel functionalities and applications of OTFTs in various domains.

Architectures of OFET

Recently, there has been a rise in popularity of OFETs, indicating that these transistors are exceeding expectations and are becoming more sought after for a wide range of large-area electronic applications. OFETs utilize the thin film transistor design, which has proven to be adaptable to materials with low conductivity. It mainly consists of three electrodes: a source, a drain, and a gate, as well as an active organic semiconducting (OSC) layer, a dielectric layer. Ordinary MOSFETs and OFETs are fundamentally different structurally in that the latter do not have a body terminal, making them resistant to the body effect (Figure 1).[8,9]

Depending on where the source/drain and gate contacts are in respect to the OSC layer, a variety of OFET structures can be designed.

One may place the patterned source/drain electrodes before or after the organic semiconductor (OSC) deposition. The first arrangement is called "coplanar" and also called "bottom contact," whereas the second configuration is called "staggered" and also called "electrode contact at top". Bottom and top gate structures are included in the coplanar and staggered designs. Even with the identical materials, the different FET layouts can exhibit dramatically different device characteristics. The insulator layer and source/drain contacts are on the same side of the channel in a coplanar design, but they are on the opposite side in a staggered layout (Figure 2).[2]

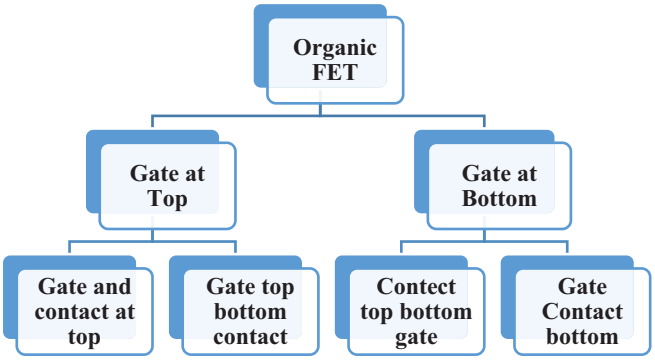

Fig 1 | Organic FET flowchart and architectures

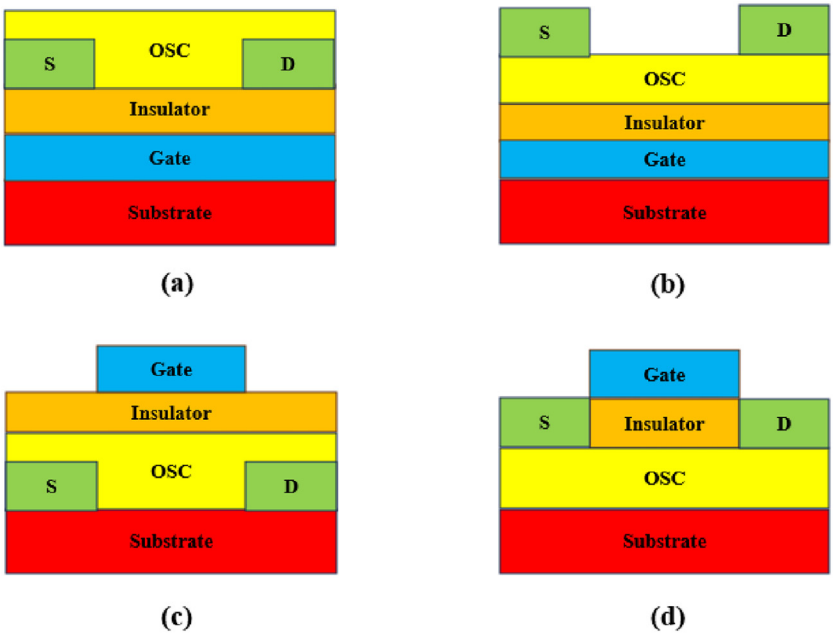

Fig 2 | (a) Device gate and contact in bottom. (b) Device gate and contact in bottom and top. (c) Device gate and contact in top and bottom. (d) Both gate and contact at top

Architecture Of BGTC

The BGTC OFET architecture represents an organic FET with a configuration that utilizes a bottom-gate and a top-contact. In this configuration, the gate electrode is positioned beneath the OSC layer, while the source and drain electrodes are situated above the OSC layer. This architectural design offers the advantage of facilitating improved contact between the OSC and the electrodes, thereby enhancing charge transport and decreasing contact resistance. The disadvantage is that it requires a careful alignment of the electrodes and the OSC layer, which can be challenging for large-area fabrication.[3,10]

Importance of TCAD Simulation

Engineers and researchers can use TCAD simulation to model and simulate the behavior of semiconductor devices at a small scale. It aids in understanding the physics and properties of devices, allowing for more efficient design and optimization. TCAD assists in identifying the ideal device characteristics and performance trade-offs by iteratively modelling alternative device architectures, material compositions, and operating circumstances. TCAD simulation gives insight into the performance of semiconductor devices prior to production. It predicts critical device parameters as current-voltage characteristics, capacitance, breakdown voltage, and switching speed. TCAD simulations support informed design decisions and help meet device specifications by accurately predicting device performance.[2,3]

TCAD simulation is critical for understanding the problems and possibilities associated with lower device dimensions due to the constant scaling of semiconductor devices. It aids in the prediction of the influence of scaling on device performance, addressing concerns like as short-channel effects, quantum mechanical effects, and device variability. To overcome scaling limits, TCAD simulations assist the development of innovative device designs and technologies.[7,10]

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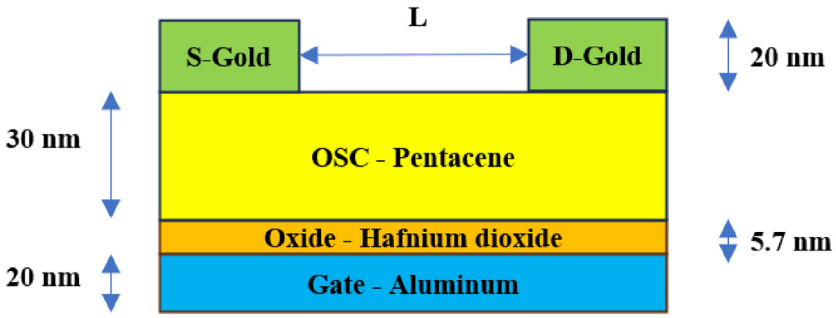

Fig 3 | Schematic view of bottom gate OFET

Table 1 | Simulation input parameters of OFET

Parameters	Material	Dimension (nm)
Electrode (Source and Drain) thickness	Gold	20
Organic semiconductor thickness	Pentacene	30
Dielectric thickness	HFO_2	5.7
Gate electrode thickness	Aluminum	20
Device channel length		30

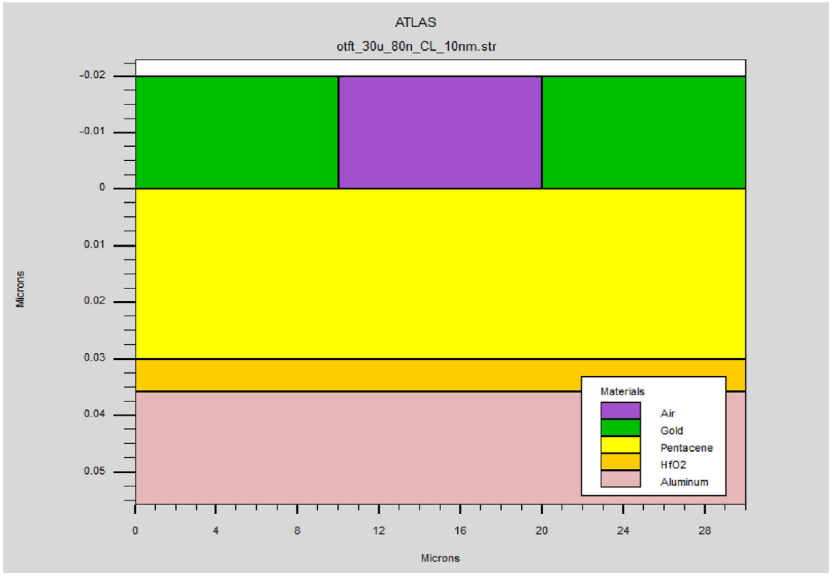

Fig 4 | Structure of the device

Device Structure

We employed an analytical model-based simulator to simulate the bottom gate with top contact structure to understand the device physics. We utilized the Silvaco Atlas 2-D numerical device simulator to explore the electrical characteristics of this configuration. The gate electrode made of aluminium has a thickness of 0.02 m (20 nm). The HFO_2 gate dielectric, which has a dielectric constant of 22.0, is positioned above the 5.7 nm-thick gate electrode.

The p-type organic semiconductor pentacene layer, which has a thickness of 30 nm and a doping concentration of 3×10^{17}, was deposited over the oxide layer to construct the conducting channel. Even though this is a simulation, similar procedures will be used when producing the genuine gadget.[11] Figure 3 depicts the BGTC OFET schematic view.

Material deposition is a technique used to assess different OFETs' performance. Spin-coating, which involves processing the polymer solutions on a substrate, is the most widely used method for creating thin polymer films. In addition, a variety of orienting techniques are employed in thin-film deposition. This involves the use of the floating film transfer method, a cutting-edge substitute for uniformly deposited, well-oriented polymer thin-film (OSC) that has been extensively used in the creation of PQT-12 polymer-based functional transistor.[12,13]

Moreover, the source and drain of the OSC's active layer have metal contacts (Au) positioned on top of them.[3] In the current study, the deposition of the source and drain electrodes is adjusted to match the structure, with a thickness of 20 nm. The dimensional parameters based on the structure, along with the material and thickness, are summarized in Table 1.

Parameters

In this paper, we are going to evaluate the behavior of some parameters with respect to the performance of OFET. The list of parameters used for understanding the operation of OFET is as follows:

- Channel Length: The channel length will be changed from 10 µm to 120 µm in increments of 10 µm, and data will be collected for all values and will make the conclusion on how the variation of channel length is affecting the performance of OFET.
- Different Dielectric Materials: We will use different dielectric materials such as Al_2O_3, HfO_2, Si_3N_4, SiO_2, and Ta_2O_5 and we will obtain the results for all materials and will make conclusion on how the variation of dielectric material is affecting the performance of OFET.[10]
- Dielectric Thickness: we will vary dielectric thickness[14] from 2 nm to 10 nm with an increment of 2 nm, 30 nm, 50 nm and we will obtain the results for all values and will make conclusion on how the variation of dielectric thickness is effecting the performance of OFET.
- Drain Voltage: we will vary drain Voltage from –1 V to –4 V with an increment of 1 V and we will obtain the results for all values and will make conclusion on how the variation of drain Voltage is effecting the performance of OFET

The Deveice

In this paper, we are implementing the bottom gate top contact OFET with the dimensions discussed in device structure. The TCAD tool used for implementing this device is Silvaco TCAD. The device's design utilized a 20 nm Al layer as the gate and a 5.7 nm HFO_2 layer as the dielectric, as depicted in Figure 3.[7,10] The source and drain contacts consisted of a 20 nm thick layer of gold on top of a 30 nm thick organic pentacene layer. The channel length measured 10 µm (Figure 4).

Results and Discussion

Channel Length

The channel length is being varied ~10 to ~120 µm with an increment of 10 µm with a drain voltage of −1 V and gate voltage is varied from 0 V to −30 V (Table 2 and Figure 5).

The device's design utilized a 20 nm Al layer as the gate and a 5.7 nm HFO_2 layer as the dielectric, as depicted in Figure 3.[7,8] The drain and source electrode consisted of a ~20 nm thick layer of gold after 30 nm thick organic pentacene layer. The channel length measured ~10 µm. From the equations we can see that if all terms are kept constant except channel length(L), we can say that drain current is inversely proportional to channel length. Hence, the conclusion from the first parameter – Channel length is that, If the channel length increases the drain current decreases.

$$I_D = \frac{W}{L}\mu C\left[(V_{GD} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$I_D = \frac{W}{2L}\mu C(V_{GS} - V_T)^2 V_{DS}$$

Dielectric Material

Our next parameter is variation of dielectric material. we used different dielectric materials such as Al_2O_3, HFO_2, Si_3N_4, SiO_2, Ta_2O_5 with a drain voltage of −1 V and gate voltage is varied from 0 V to −30 V (Table 3 and Figure 6).

From the above graph, we can say that device with Ta_2O_5 as a dielectric is having high drain current (ON Current), and the device with SiO_2 as a dielectric is having low drain current. This is because of permittivity. The device which is having high permittivity material as dielectric material will have high drain current, permittivity of Ta_2O_5 is 26.0, so it has high drain current. The device which is having Low permittivity material as dielectric material will have low drain current, permittivity of SiO_2 is 3.9, so it has Low drain current. We can say that device which is having

Table 2 | Transfer characteristics of device with different channel length's

Channel Length (µm)	Drain Voltage (V)	Drain Current (A)
10	−1	−1.05E-12
20	−1	−5.57E-13
30	−1	−3.80E-13
40	−1	−2.88E-13
50	−1	−2.31E-13
60	−1	−1.94E-13
70	−1	−1.66E-13
80	−1	−1.46E-13
90	−1	−1.30E-13
100	−1	−1.17E-13
120	−1	−9.77E-14

Table 3 | Transfer characteristics of device with different dielectric materials

Dielectric Material	Drain Voltage (V)	Drain Current (A)
Al_2O_3	−1	−4.64E-13
HfO_2	−1	−1.05E-12
Si_3N_4	−1	−3.78E-13
SiO_2	−1	−2.01E-13
Ta_2O_5	−1	−1.23E-12

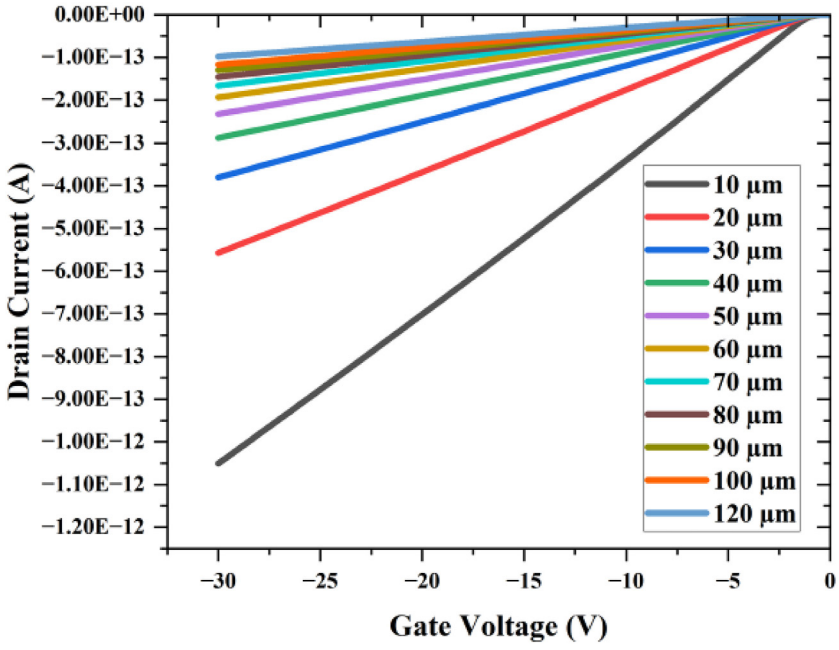

Fig 5 | Comparison plot of transfer characteristics of device with different channel length's

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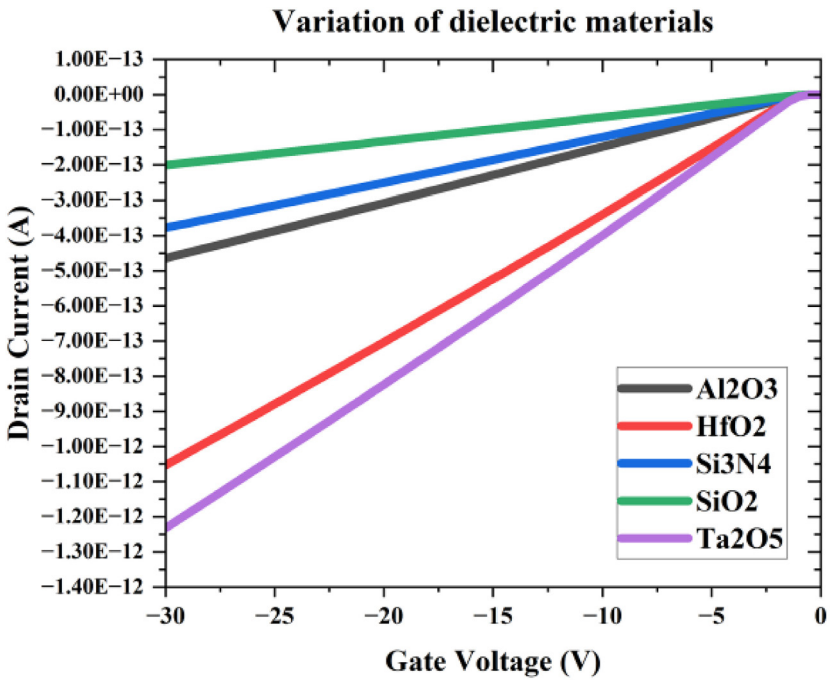

Fig 6 | Comparison plot transfer characteristics plot of the device with different dielectric materials

Table 4 | Permittivity values of different dielectric materials

Dielectric Materials	Permittivity
SiO_2	3.9
Al_2O_3	8.5
Si_3N_4	7.5
Ta_2O_5	26.0
HfO_2	22.0

Table 5 | Transfer the characteristics of device with different dielectric thickness

Dielectric Thickness (nm)	Drain Voltage (V)	Drain Current (A)
2	−1	−2.78E-12
4	−1	−1.47E-12
6	−1	−1.00E-12
8	−1	−7.64E-13
10	−1	−6.18E-13
30	−1	−2.15E-13
50	−1	−1.31E-13

high permittivity material as dielectric will produce high drain current. The permitivities of materials used as dielectric in above devices are shown in below figure (Table 4).

Dielectric Thickness

The third parameter is variation of dielectric thickness. we varied dielectric thickness from 2 nm to 10 nm with an increment of 2 nm, 30 nm and 50 nm with a drain voltage of −1 V and gate voltage is varied from 0 V to −30 V (Table 5 and Figure 7).

The plot above indicates that the drain current decreases as the dielectric layer thickness increases. As a result, a greater drain current is seen at lower oxide thickness, which improves the sub-threshold swing and switching on/off ratio. At lower dielectric thickness, however, the threshold voltage is higher than at higher dielectric thickness.

Drain Voltage

The final parameter is drain voltage. we varied drain Voltage from −1 V to −4 V with an increment of 1 V with a drain voltage of −1 V and the gate voltage varied from 0 V to −30 V and we obtained the results for all values. Since we are changing the drain voltage, which is an internal parameter, variation of drain voltage will not affect the structure of the device (Table 6 and Figure 8).

We can see the transfer curves of device at different drain voltages. We are getting the best result/best drain current at $V_d = -2$ V.

Conclusion

The paper encompasses the findings and insights gained from varying four key parameters. Valuable insights have been gained about how these parameters affect the performance and characteristics of the OFET through simulation. Firstly, by varying the channel length, it was observed that shorter channel lengths resulted in higher drain currents and improved switching characteristics. This finding indicates that reducing the channel length can enhance the overall performance

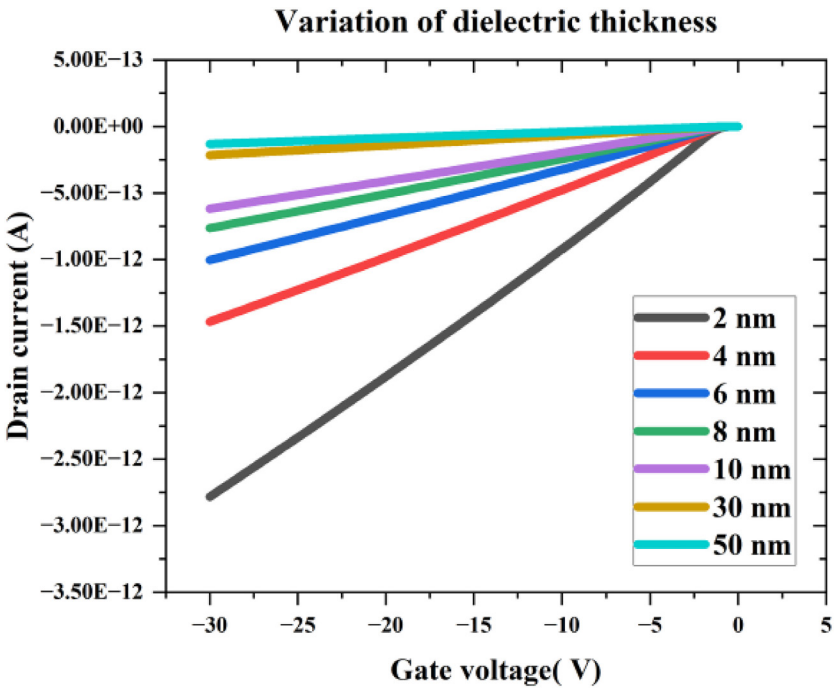

Fig 7 | Comparison plot of transfer characteristics plot of device with different dielectric thickness

Table 6 | Transfers characteristics of device with variation of drain current

Drain Voltage (V)	Drain Current (A)
−1	−1.05E-12
−2	−4.92E-12
−3	−3.06E-12
−4	−2.07E-12

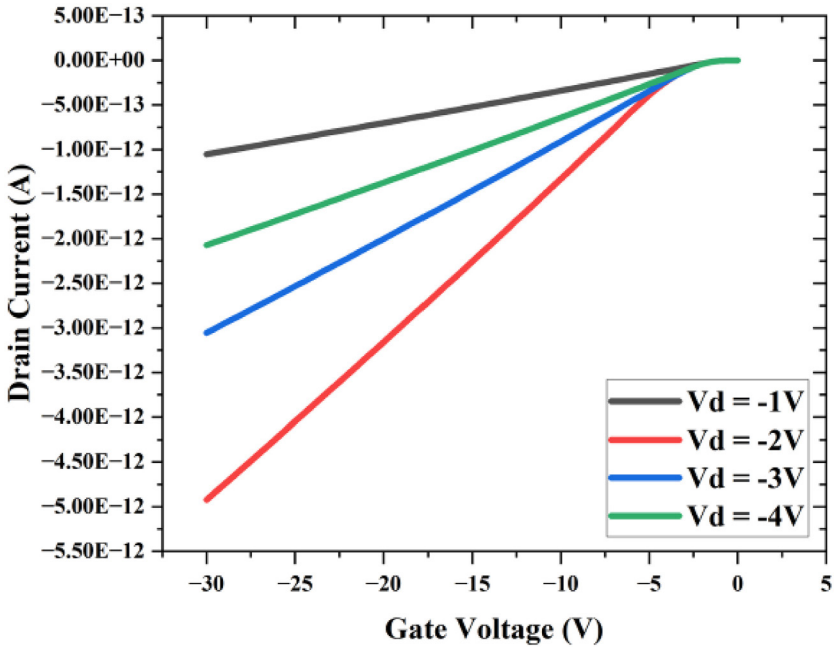

Fig 8 | Comparison plot of transfer characteristics of devices with different V_d

of the OFET, leading to faster operation and improved device efficiency. Hence, the Channel length is inversely proportional to drain current. Secondly, by varying different dielectric materials, is observed that usage of Ta_2O_5 as dielectric produced high drain current and usage of SiO_2 as dielectric produced Low drain current. This is because, Ta_2O_5 has high Permitivity and SiO_2 has low Permitivity. As a result, materials with high permittivity aid in achieving high oxide capacitance, and therefore the drain current value is increased. Thirdly, the device characteristics were determined to be significantly influenced by the thickness of the dielectric, which was found to be a critical parameter. The device which has 2 nm dielectric thickness has high drain current. Varying the dielectric thickness demonstrated that thinner dielectric layers improved the device's switching speed and produced high drain current. This outcome highlights the importance of carefully selecting the dielectric thickness to optimize the performance of the OTFT. Lastly, the overall behavior of the OTFT was significantly influenced by the drain voltage. By varying the drain voltage, it was observed that different operating regions, such as the saturation and linear regions, could be achieved. Adjusting the drain voltage allowed for controlling the device current and optimizing the device's operational range.

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